**Comparative Analysis of Partial Product Addition in Vedic UrdhvaTiryakbhyam Multiplier**

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***Abstract***

*Multiplication is one of important operation performed in many Digital signal processing applications. Hence the performance of the multiplier will affect the overall performance of the DSP processor. The methods like booth multiplier, array multiplier are used. Vedic multiplication technique had proved its importance in getting the speed of multiplication. It is required to add the generated partial products quickly, to generate the result of multiplication faster. To add the generated partial products different schemes are used such as ripple carry adders, carry look-ahead adders, carry save adders etc. This paper aim to use the UrdhvaTiryakbhyam method of vedic multiplication and present the comparison of different partial product addition methods. The comparison shows that the proposed method with half adders and full adders is better alternative if little increase in propagation delay is accepted at the cost of reduced area i.e. slices and LUTs the proposed method of half adders and full adders is better choice for addition of partial products. Also the power dissipation of this method is less as compared to other methods.*

***Keywords****: Vedic mathematics, UrdhvaTiryakbhyam multiplier, Partial Products(PP) Ripple Carry Adder (RCA), Carry Look-ahead Adder (CLA).*

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**INTRODUCTION:**

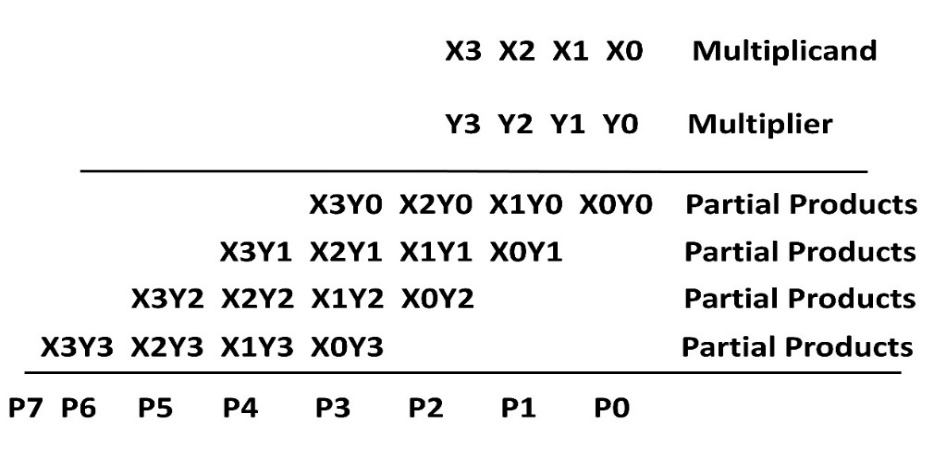
Multiplication of the input signals is required for linear filtering, frequency domain processing with FFT, voice or image processing application, encryption, and decryption. DSP processors with multiplier blocks carry out this multiplication. The effectiveness of the multiplier block is critical element in determining the performance of the entire system. The shift and add approach is the basic for the hardware implementations of standard array multipliers. Half adders and full adders are used in this method to sum the partial products; however, the performance is low due to a significant propagation delay in carry propagation. It's essential to add the partial products with a shorter propagation delay in order to increase speed of the multiplication. Use of Vedic mathematics methods will give the better results.

Sri Bharti Krishna Tirathaji developed the Vedic sutras between 1911 and 1918 [1]. There are 16 primary sutras; UrdhvaTiryakbyham is the most popular of these. The method of UrdhvaTiryakbyham will be the better option, the performance of these multiplier can be verified using hardware description language(HDL) and implementing them on the reconfigurable hardware. N×N multiplication [2-3] applicable for 4,8,16 and 32-bit multiplication is explained. This method requires not as much of computation time for finding the multiplication output for N×N bit. Vedic UrdhvaTiryakbyham [4] multiplier implemented using FPGA and ASIC. For implementation they used ASIC design based on standard cell, with which vedic multiplier is implemented in 180 nm CMOS technology, This resulted in speed of 5.2 ns, power 257 µW, and it is using area of 1,117 cells. UrdhvaTiryakbyham multiplier is effectively implemented for decimal number system [5], complex number system [6] and floating point numbers [7-8]. The advantage of power dissipation of the reversible logic [9-11] and adiabatic logic [12-13] is successfully utilized in Vedic multiplier to reduce the power and design of low power high speed Vedic multiplier.

In order to increase the speed of multiplication it is required to add the partial product quickly. The use of increment by one (IBO) block along with carry save adder [14] and modified adder [15] resulted in reduced delay in multiplication. As adding these partial products with less delay is important, many researchers have used carry save adders [16], carry lookahead adders [17], carry select adder [18], multiplexer based adders [19-20], barrel shifter [21] and arithmetic adders [22] to improve the delay in multiplication. The partial product addition schemes [23] are compared for area, delay and power. This paper presents the comparison of different methods of partial products addition in Vedic UrdhvaTiryakbyham multiplier along with the proposed hierarchical arrangement of multiplication using half adders and full adders.

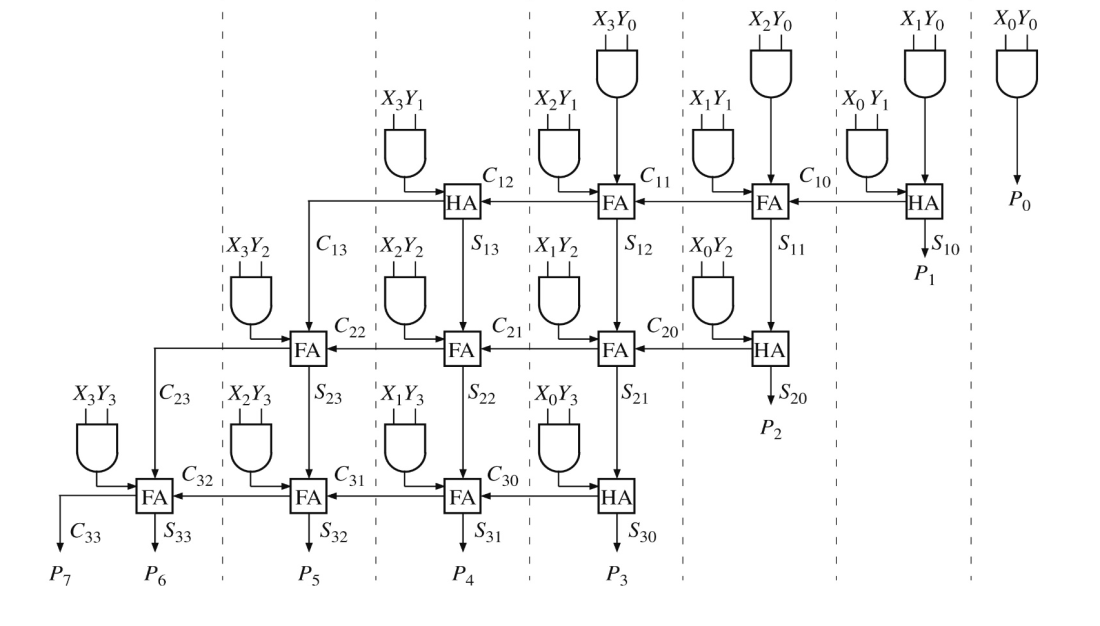
**ARRAY MULTIPLIER:**

The multiplication any two numbers are performed by following procedure for binary numbers which is similar to decimal numbers.



***Fig. 1:*** *4 × 4 Bit Multiplier*

In figure 1 each partial product term e.g. X0Y0, X1Y0… represents a bit which is result of bit by bit multiplication. This bit by bit multiplication is performed with the help of AND gate. As the array multiplier is based on simple shift and add multiplication. All the partial products are added with the full adders and half adders as shown in figure 2 for the 4×4 bit multiplication



***Fig. 2:***  *4 × 4 Bit Array Multiplier*

This 4×4 bit array multiplier is shown in Fig. 2 uses AND gates for bit by bit multiplications. For 4×4 bit multiplication sixteen AND gates are required. Each row of 4 AND gates form one row of partial products, these partial products are added using full adders and half adders. The bits P7 to P0 are 8 result bits shown in Fig. 2. For 4×4 bit multiplication it needs 4 half adders and 8 full adders.

Similar scheme of array multiplier is used for 8 and 16 bit multiplication. The 8 bit multiplier will require 8 half adders and 48 full adders whereas 16 bit array multiplier will use 16 half adders and 244 full adders.

**VEDIC URDHVATIRYAKBHYAM MULTIPLIER:**

Vedic Multiplier based on UrdhvaTiryakbhyam (Vertical and Crosswise) performed using following procedure. The 2×2 bit multiplication will produce the result of 4 bits. The multiplier is A=A1A0 and multiplicand is B=B1B0. Let the result is “P3P2P1P0”.

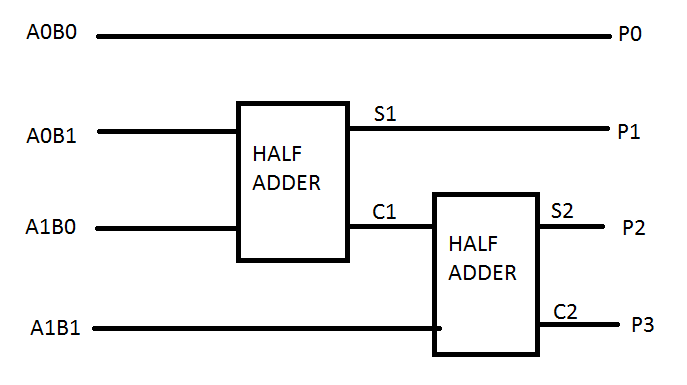
P0= A0B0

C1P1=A1B0 + A0B1

C2P2=A1B1 + C1

P3=C2

The above procedure of vedic multiplier can be implemented using 2 half adders as shown in Fig. 3



***Fig. 3:*** *2×2 Bit Vedic Multiplier With Half Adders*

## **URDHVATIRYAKBHYAM VEDIC MULTIPLIER WITH RCA ADDERS:**

The 4 x 4 bit multiplication can be performed as, let the multiplier is A3A2A1A0 and the multiplicand is B3B2B1B0 by following the procedure of Urdhva-Tiryakbhyam multiplier the result will be of 8 bits which is represented by P7…P0. The partial products of this UT multiplier are shown in Fig. 4



***Fig. 4:*** *4* × *4 Bit Multiplication With Urdhva-Tiryakbhyam*

P0= A0B0

C1P1=A1B0 + A0B1

C3C2P2=A2B0 + A1B1 + A0B2 + C1

C5C4P3=A3B0 + A2B1 + A1B2 + A0B3 + C2

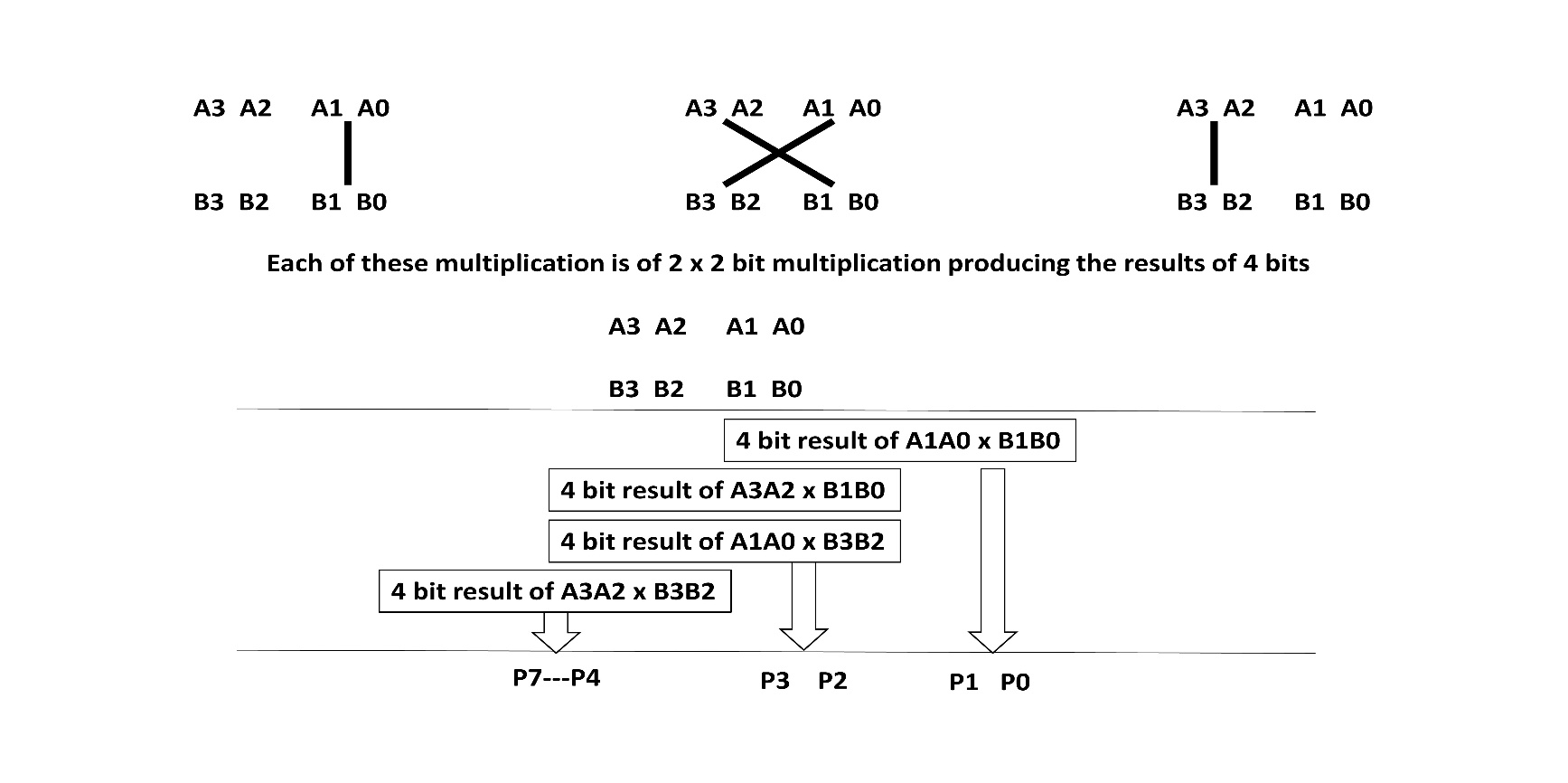
C7C6P4 = A3B1 + A2B2 + A1B3 +C3 + C4

C9C8P5=A3B2 + A2B3 +C5 +C6

C10P6=A3B3 + C7 +C8

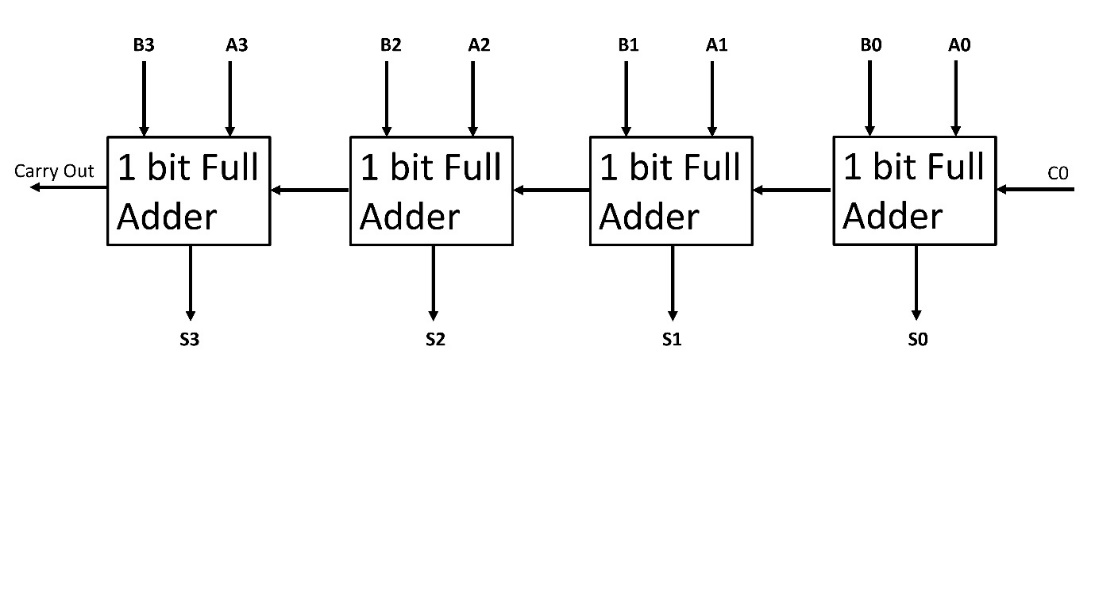
P7=C9 +C10

In this work the hierarchical approach is used. The 4×4 bit multiplication is performed by grouping 2 bits multipliers and 2 bit multiplication by Urdhva-Tiryakbhyam multiplier as shown in Fig. 5



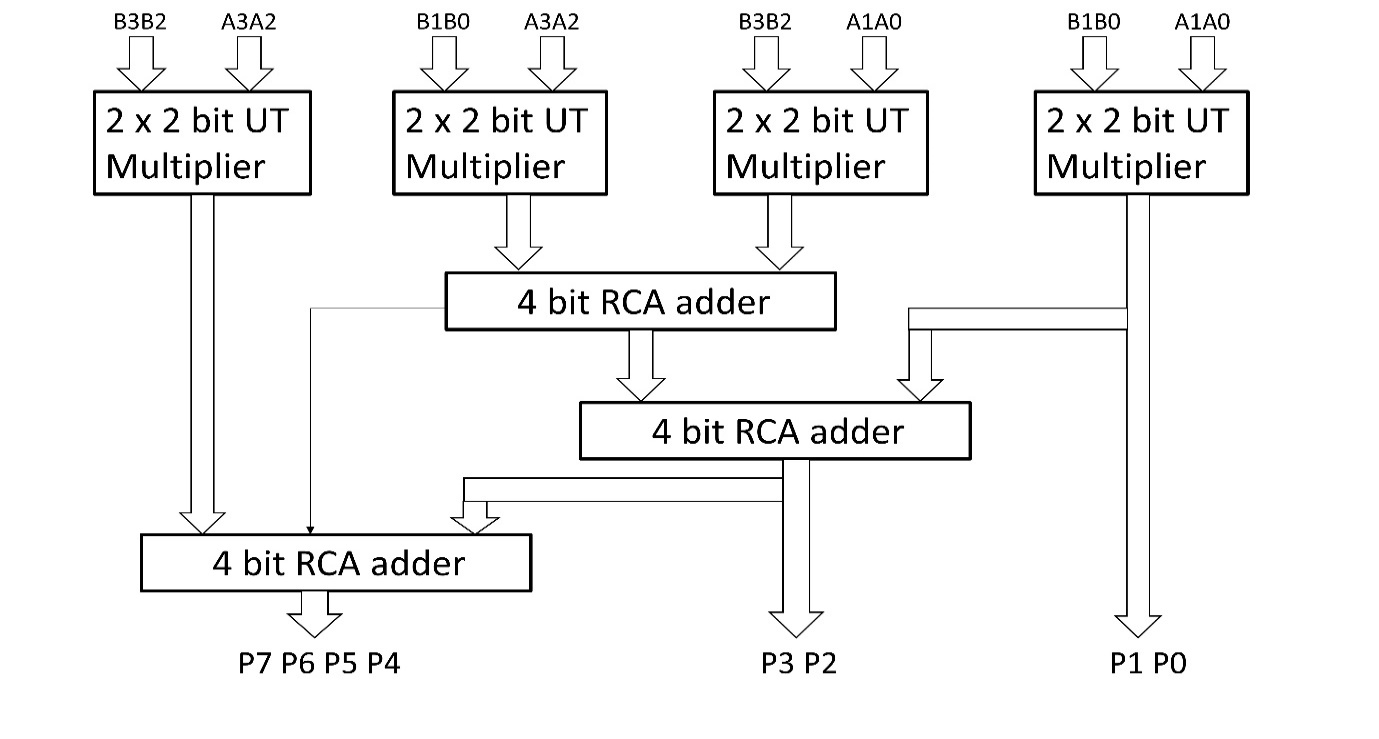
*Fig. 5: 4×4 Bit Multiplier Using Four 2×2 Bit Multiplication*

The partial product of the Fig. 5 are added with the help of 4 bit ripple carry adder (RCA) adder. The design of 4 bit ripple carry adder (RCA) is shown in Fig. 6.



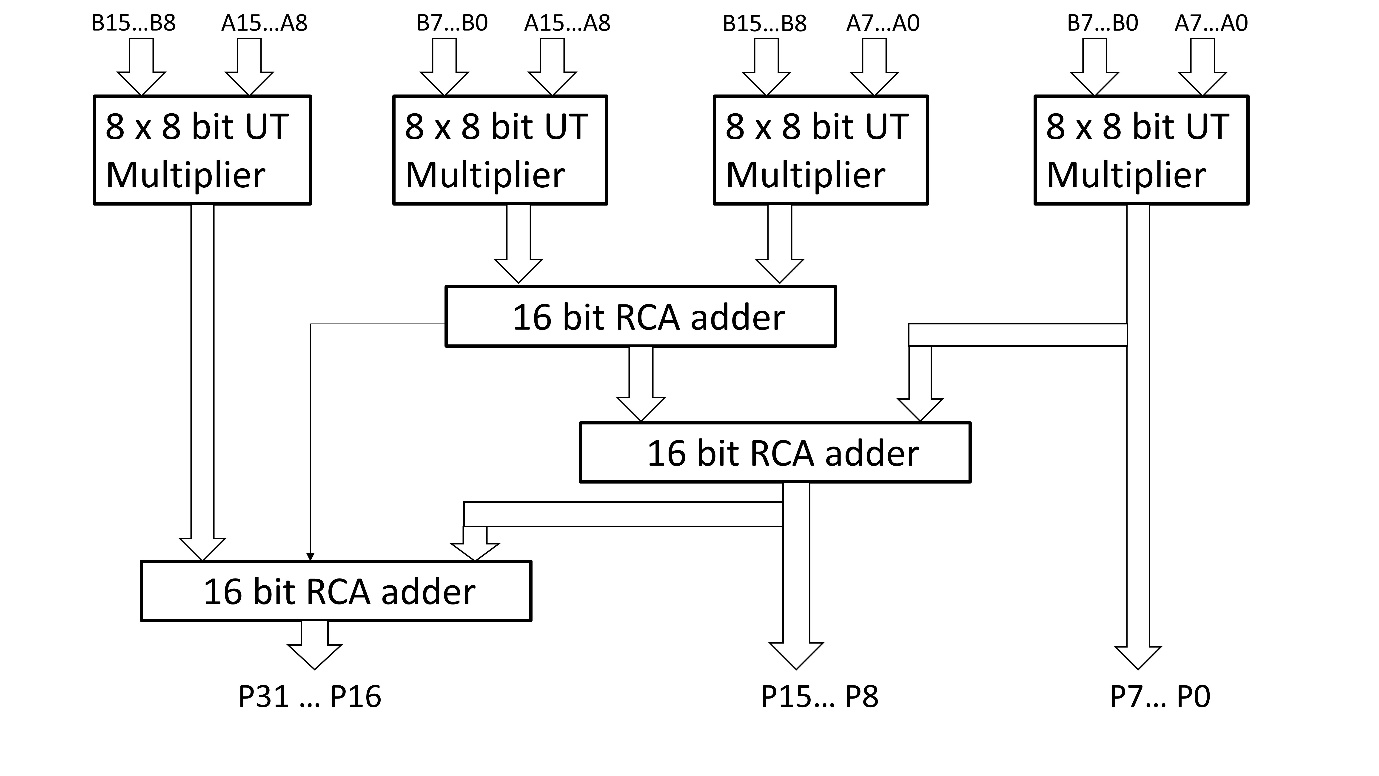
***Fig. 6:*** *4 Bit Ripple Carry Adder (RCA)*

The method of multiplication by using the RCA adder is shown in Fig. 7. Here Multiplier and multiplicand are shown by A3 A2 A1 A0 and B3 B2 B1 B0. The output bits are as P7, P6, P5, P4, P3, P2, P1 and P0.



***Fig. 7:*** *4×4 Bit Multiplier Using Four 2×2 Bit Multiplier and 4 Bit RCA Adder*

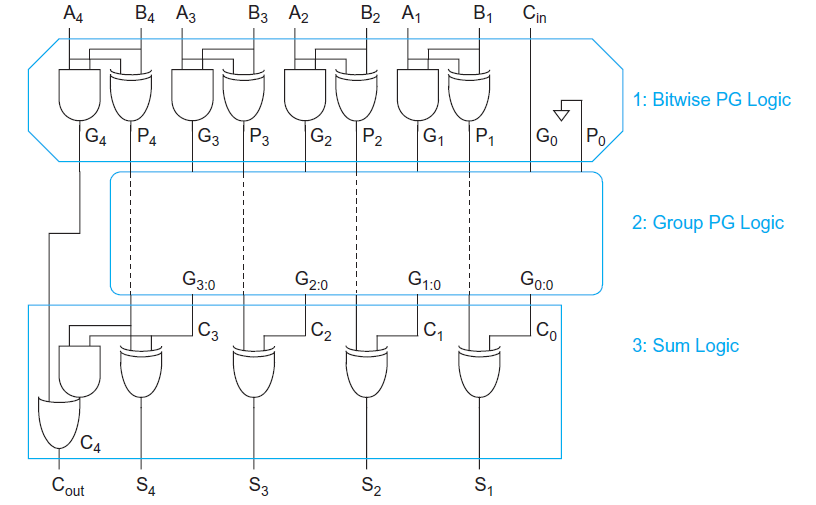
Out of the 4 bits produced by the 2 bit multiplier block of A1A0 × B1B0, 2 bits will be the result bits and the remaining 2 bits will be carry bits for the following block. The next adder will combine the carry from the preceding 2 bit multiplication with the partial products of the 2 bit multiplications A3A2 × B1B0 and A1A0 × B3B2. The carry produced by this addition will be combined with the output of A3A2 × B3B2 two-bit multiplication. Similar scheme is used for implementation of 8 × 8 bit and 16×16 bit multiplication which require three 8 bit and 16 bit ripple carry adders(RCA) to add the partial products as shown in Fig. 8.



***Fig. 8:*** *16×16 Bit Urdhvatiryakbhyam Vedic Multiplier With RCA*

## **UT VEDIC MULTIPLIER WITH CARRY LOOKAHEAD ADDER (CLA):**

For fast addition of partial products, we used the carry look ahead adders so that the delay can be further be improved. The 4 bit UT multiplier with CLA adders is designed with 2 bit multipliers and 4 bit carry look ahead circuit is shown in Fig. 9



***Fig. 9:*** *4 Bit Carry Look Ahead Adder (CLA)*

Where

P1= A1 XOR B1

G1= A1 AND B1

S1= A1 XOR B1 XOR C0 = P1 XOR C0

P2= A2 XOR B2

G2= A2 AND B2

S2= A2 XOR B2 XOR C1 = P2 XOR C1, where C1=A1 AND B1

P3= A3 XOR B3

G3= A3 AND B3

S3= A3 XOR B3 XOR C2 = P3 XOR C2, where C2= G2 or (P2 AND G1);

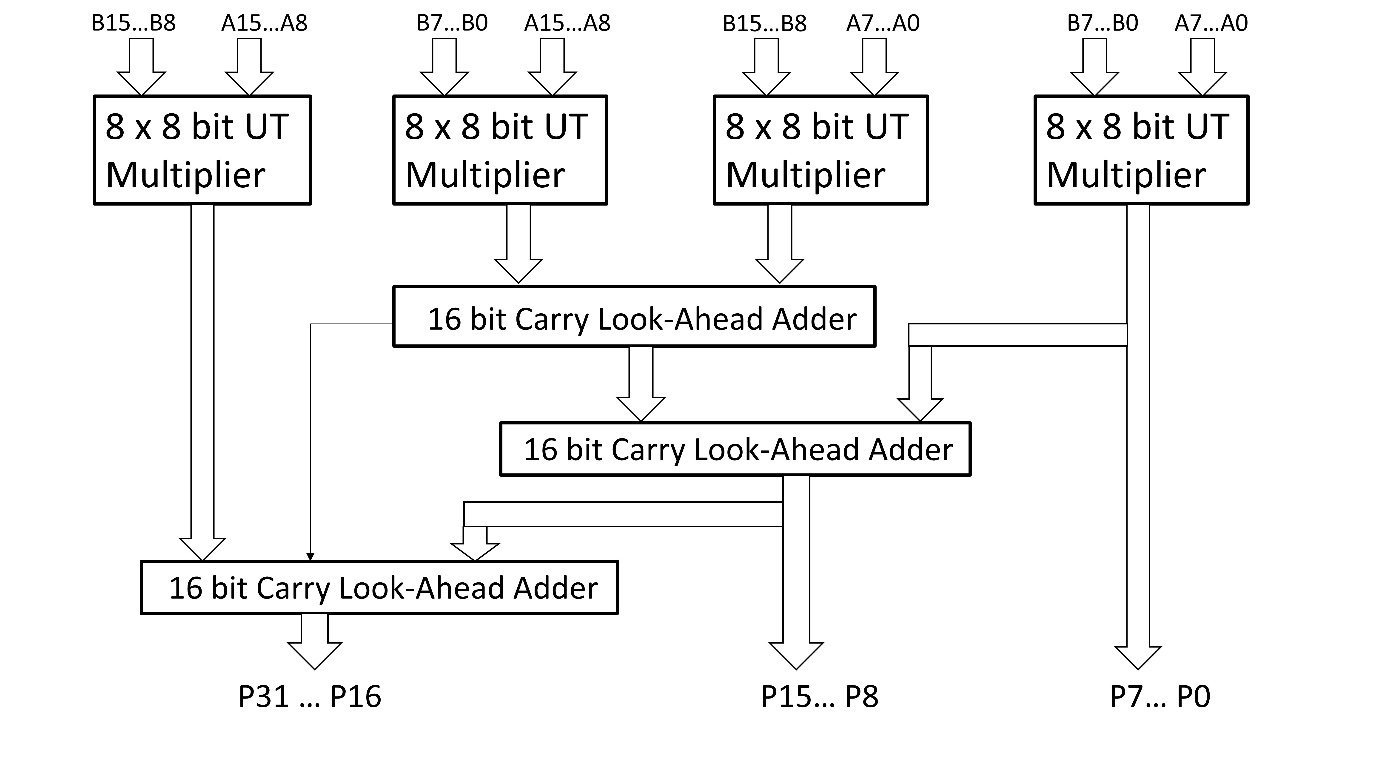
P4= A4 XOR B4

G4= A4 AND B4

S4= A4 XOR B4 XOR C3 = P4 XOR C3, where C3= G3 or (P3 AND G2 ) or (P3 AND P2 AND G1);

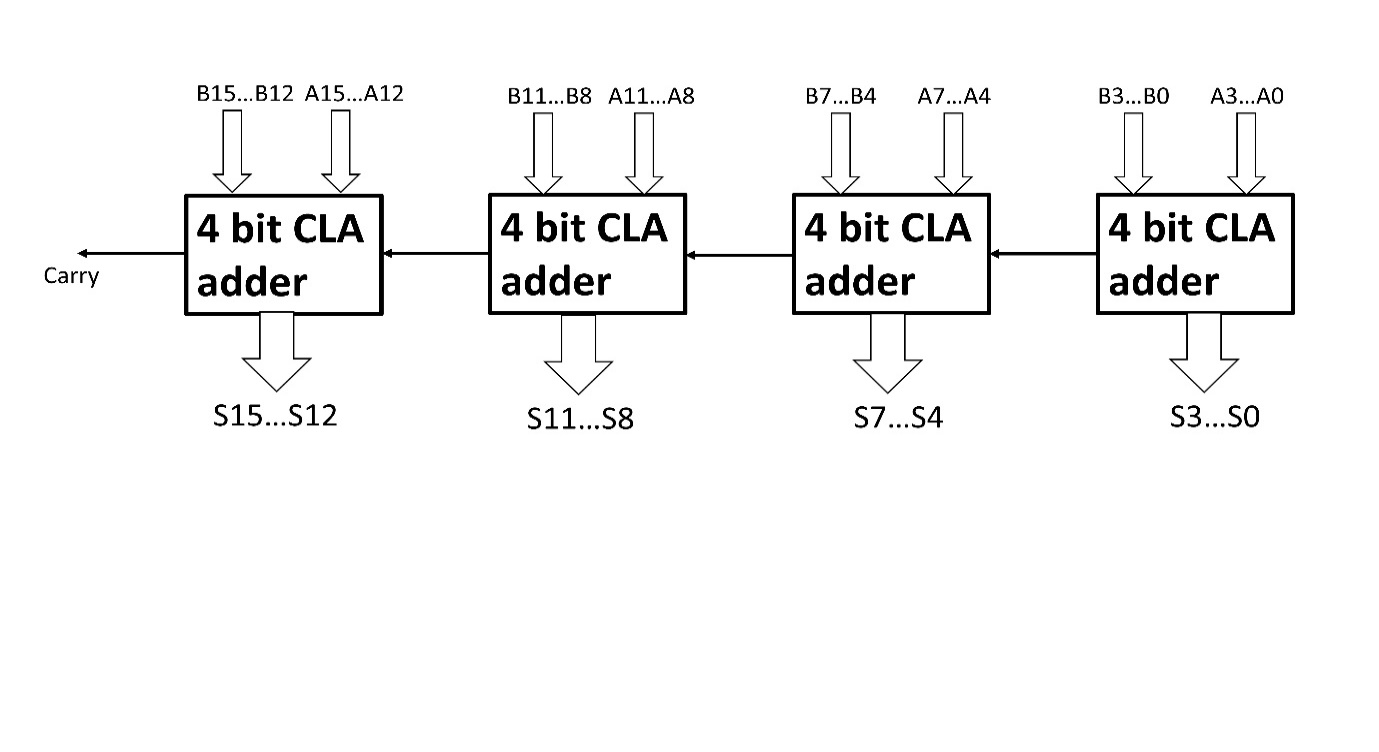
Final carry out C4= G4 or (P4 AND G3 ) or (P4 AND P3 AND G2 ) or (P4 AND P3 AND P2 AND G1)

The 16×16 bit vedic multiplier with carry look ahead adders is shown in Fig. 10. This implementation of carry look ahead adder requires complex carry generate and carry propagate logic shown in Fig. 9.

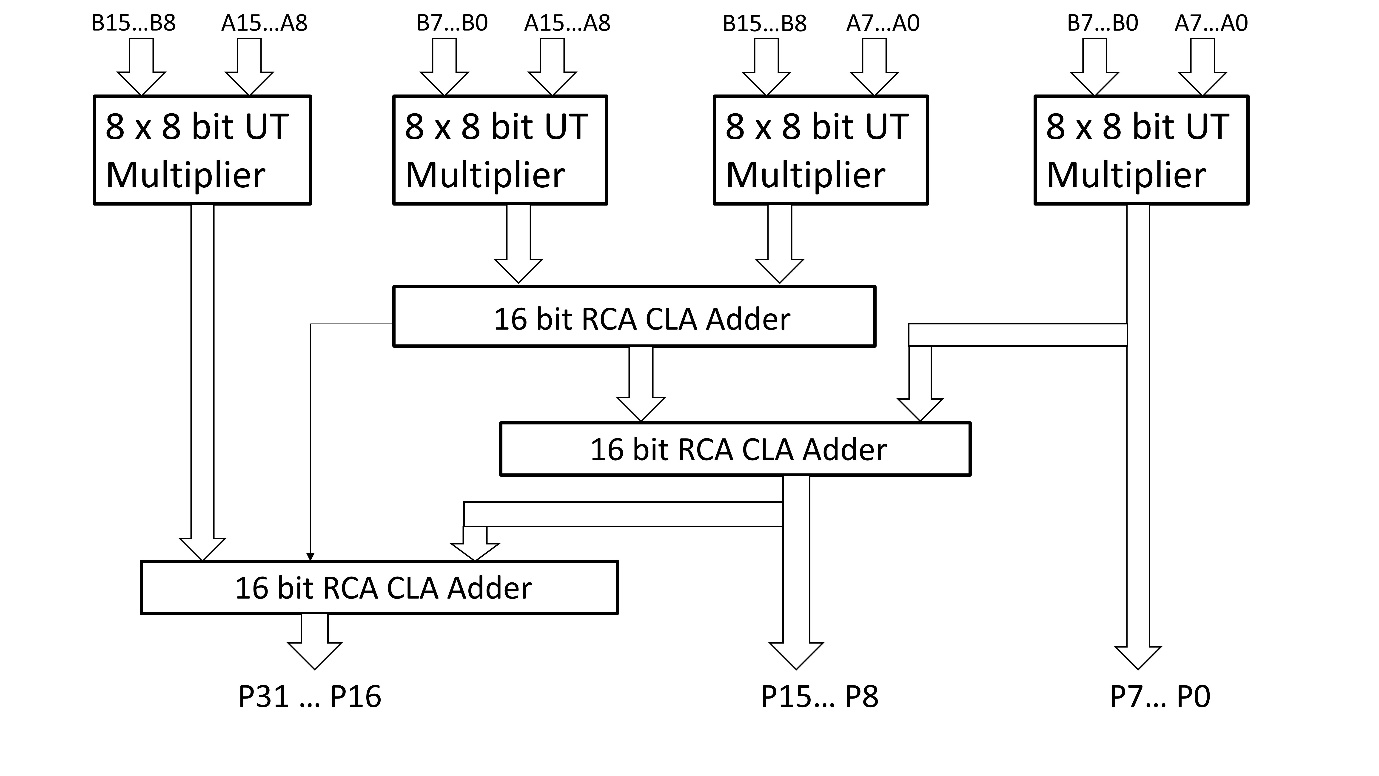
***Fig. 10:*** *16×16 Bit Vedic UrdhvaTiryakbhyam Multiplier With CLA*

**UT VEDIC MULTIPLIER WITH RCA CLA ADDERS:**

The implementation of carry look ahead adder requires complex carry generate and carry propagate logic if numbers of bits are increased. To decrease the complexity of CLA adder the RCA adder technique is used for group of 4 bit CLA adder. This adder is used in place of 16 bit CLA adder and named as 16 bit RCACLA adder as shown in Fig. 11. In this method instead of using the RCA adder or CLA adder to add the generated partial product the grouping for 4 bit CLA adder is used. For 4 bit multiplication there is no change in the implementation it is similar to the CLA adder. For 8 and 16 bit multiplication the required 8 bit and 16 bit adder is designed by the scheme shown in Fig. 11. The RCA CLA adder is used in the 16 x 16 bit UrdhvaTiryakbhyam multiplier to add the generated partial products as shown in Fig. 12.



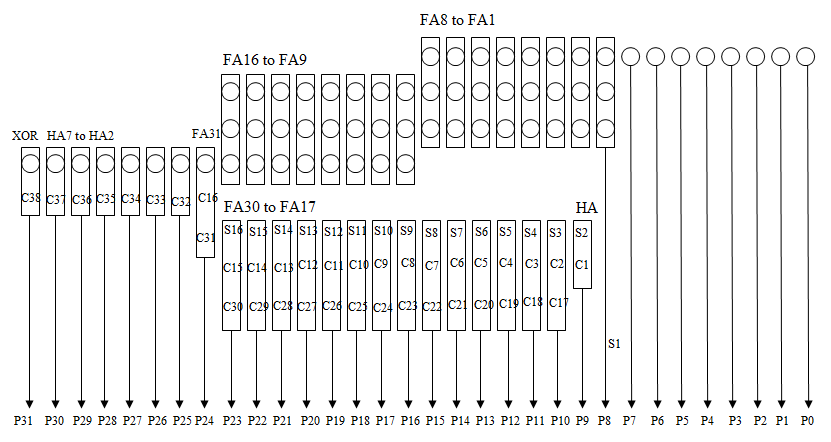
***Fig. 11:*** *16 Bit RCA CLA Adder*



***Fig. 12:*** *16×16 Bit Vedic UrdhvaTiryakbhyam Multiplier With RCA CLA Adder*

## **UT VEDIC MULTIPLIER WITH HALF ADDERS & FULL ADDERS:**

Vedic multipliers implemented with UrdhvaTiryakbyham sutras are having cascade structure. To implement 4×4 bit multiplier four 2×2 multiplier blocks are used and three 4 bit adders are used to add partial products. Similarly, to implement 16×16 bit multiplier four 8×8 bit multiplier blocks are used and three 16 bit adders are used to add partial products. The use of three RCA adders for partial products addition may lead to more delay in output. In proposed method the arrangement of half adder and full adder is used add partial products for improvement in delay, area and power. The use of RCA adders in 16 bit multiplier internally uses 48 full adders but the arrangement of half adder and full adder shown in Fig.13 uses 31 full adders, 7 half adders and XOR gate.



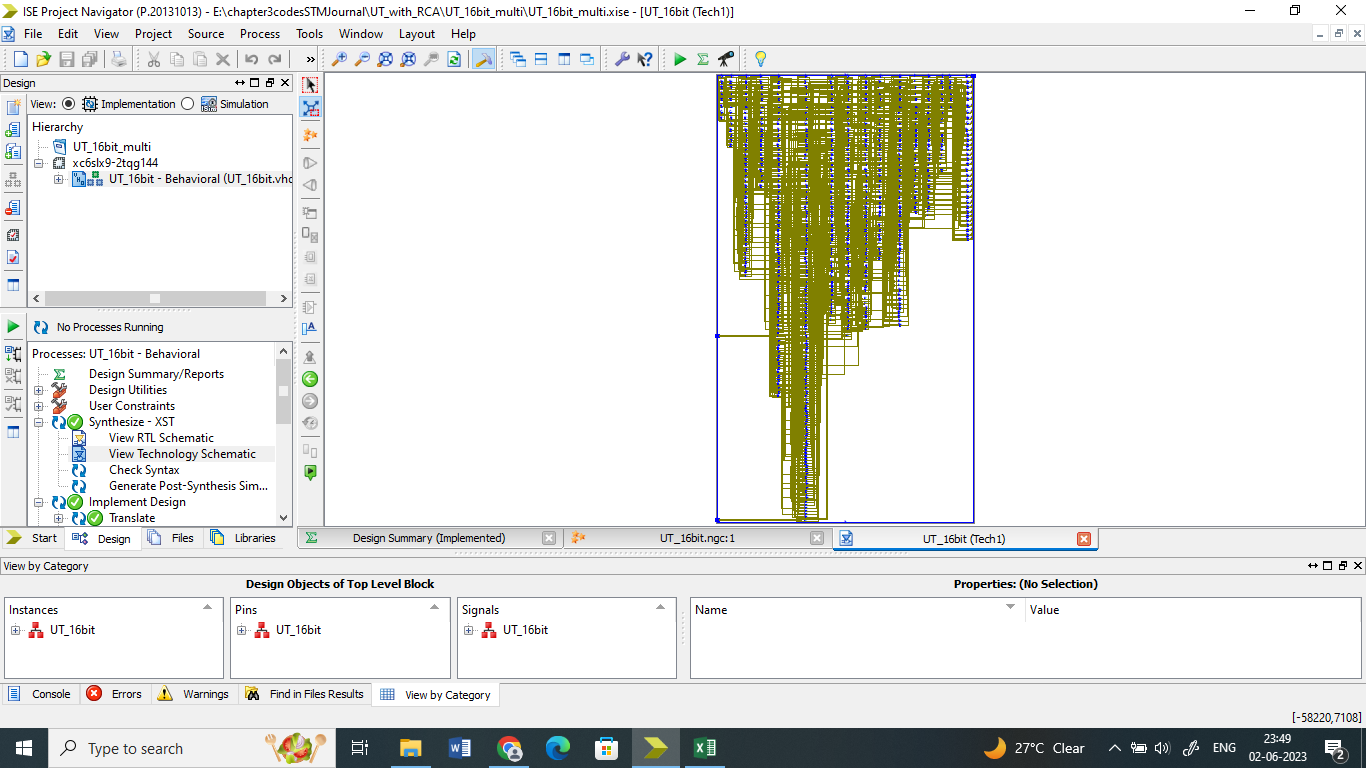
***Fig. 13:*** *16×16 Bit UT Vedic Multiplier With HA And FA*

**IMPLEMENTATION:**

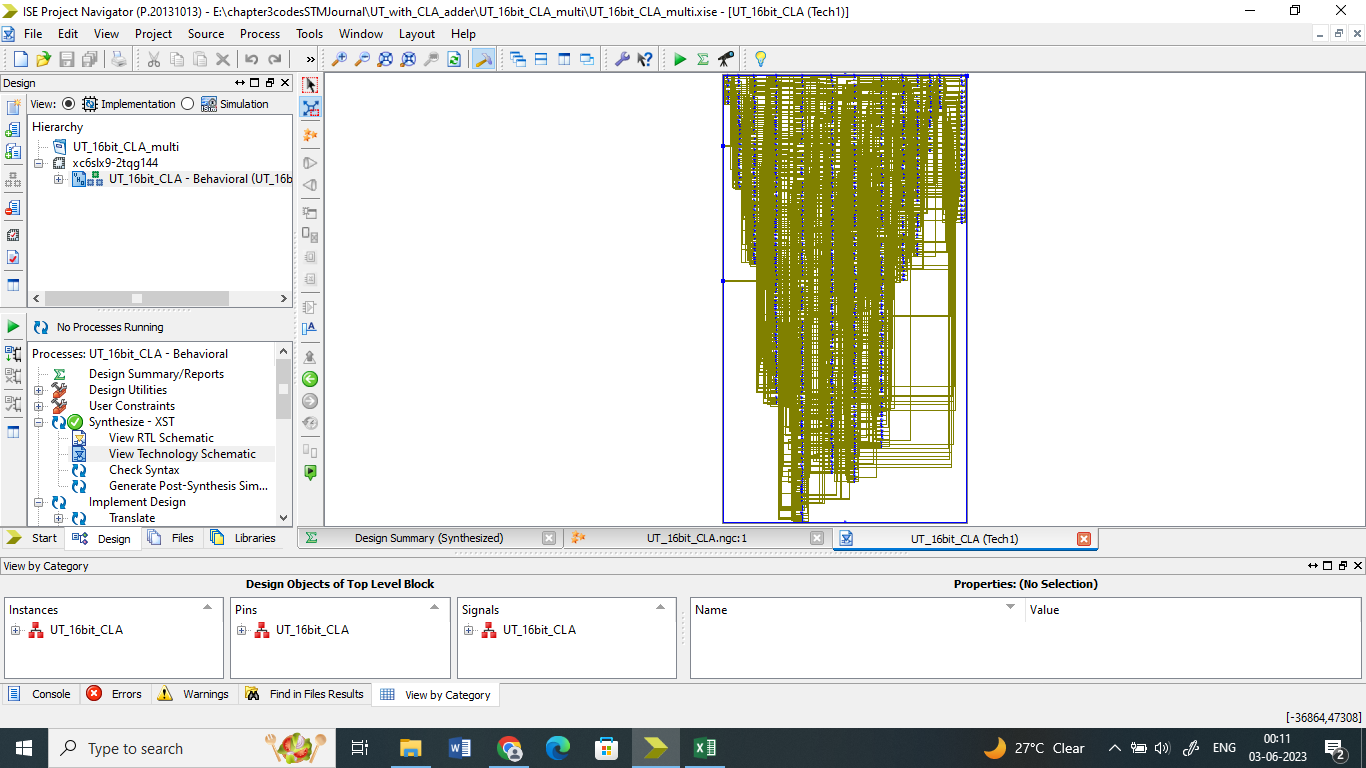
The array multiplier and vedic multipliers with ripple carry adders, carry lookahead adders and with half & full adders are implemented. These are implemented in Xilinx ISE 14.7 with VHDL code. The code for above design of multipliers written in structural modeling style. The VHDL code is synthesized using Xilinx Synthesis Tool (XST). The synthesized circuit is shown for all designs form Fig. 14 to Fig. 18.



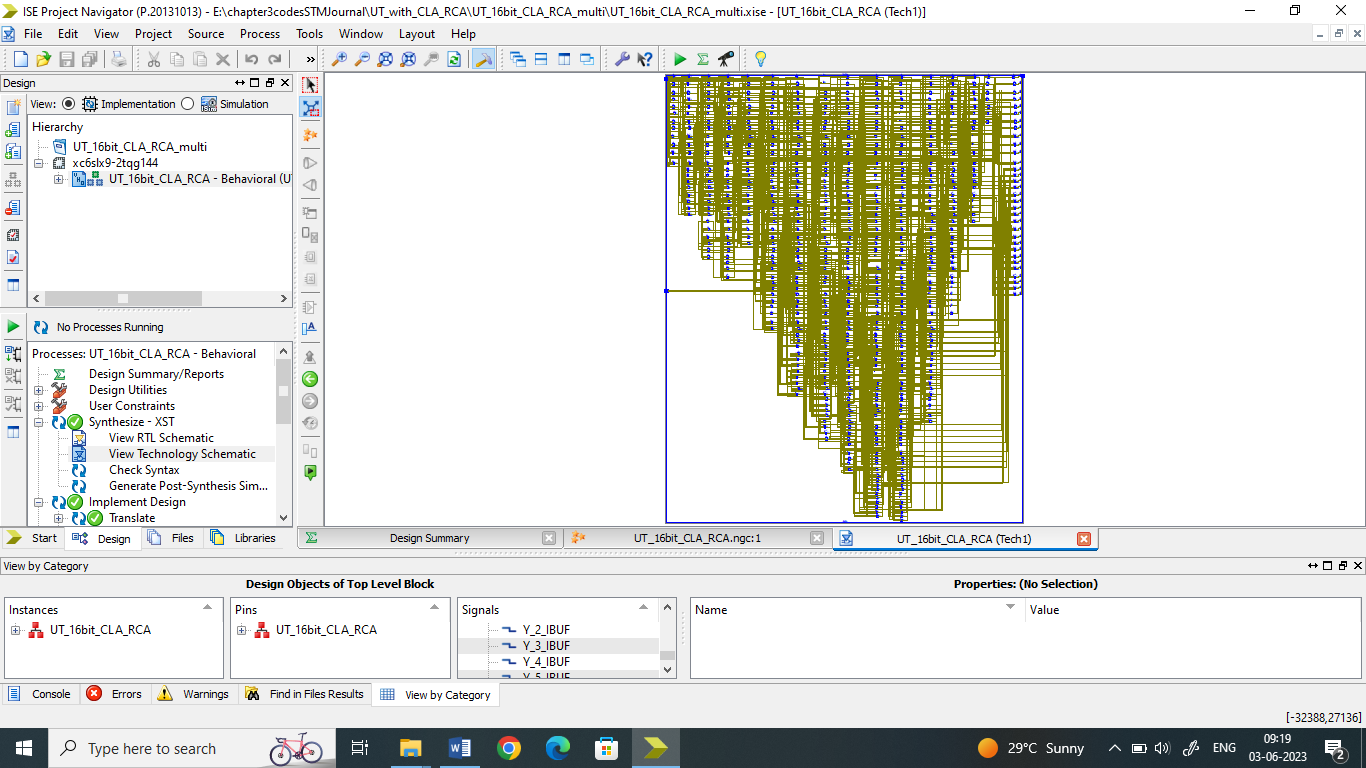
***Fig. 14:*** *Synthesis of 16×16 Bit Array Multiplier*



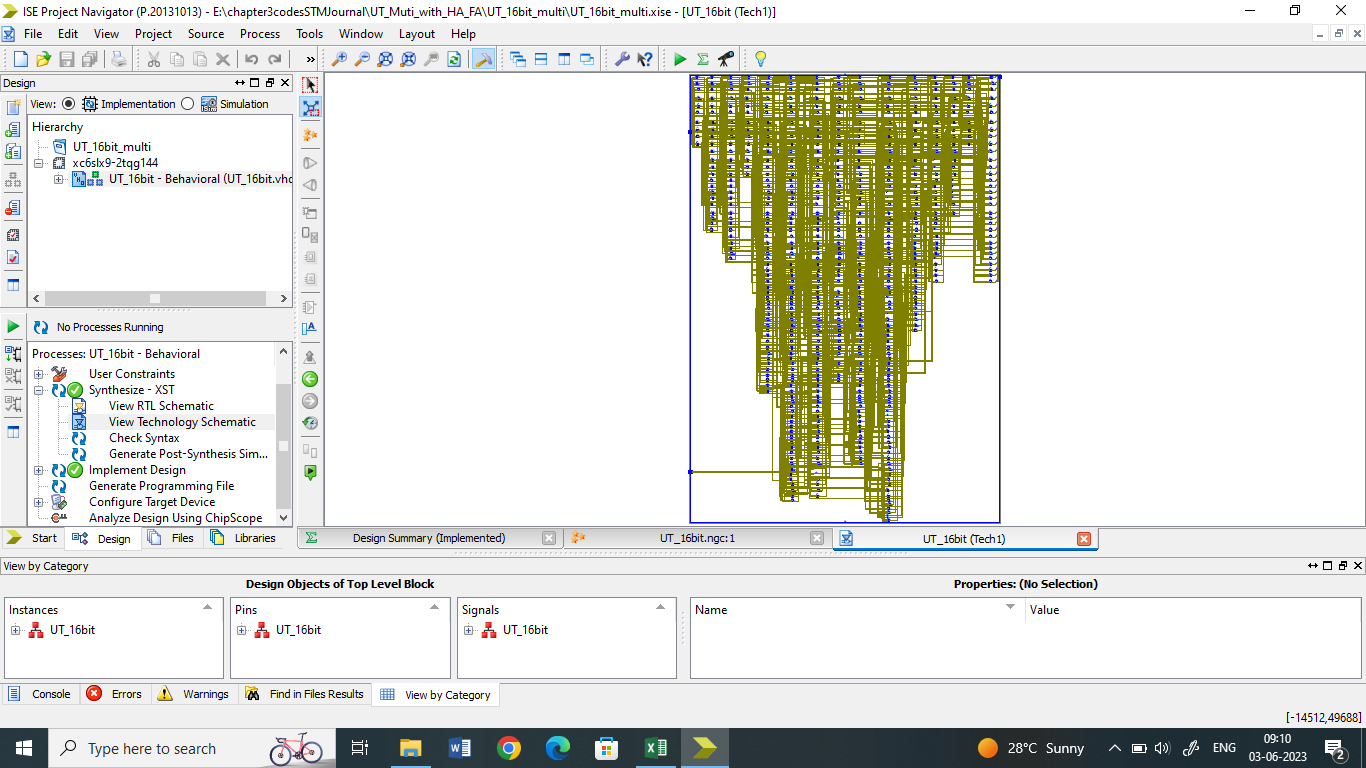
***Fig. 15:*** *Synthesis of 16×16 Bit Vedic UrdhvaTiryakbhyam Multiplier with RCA*



***Fig. 16:*** *Synthesis of 16×16 Bit Vedic UrdhvaTiryakbhyam Multiplier with CLA*



***Fig. 17:*** *Synthesis of 16×16 Bit Vedic UrdhvaTiryakbhyam Multiplier with CLARCA*

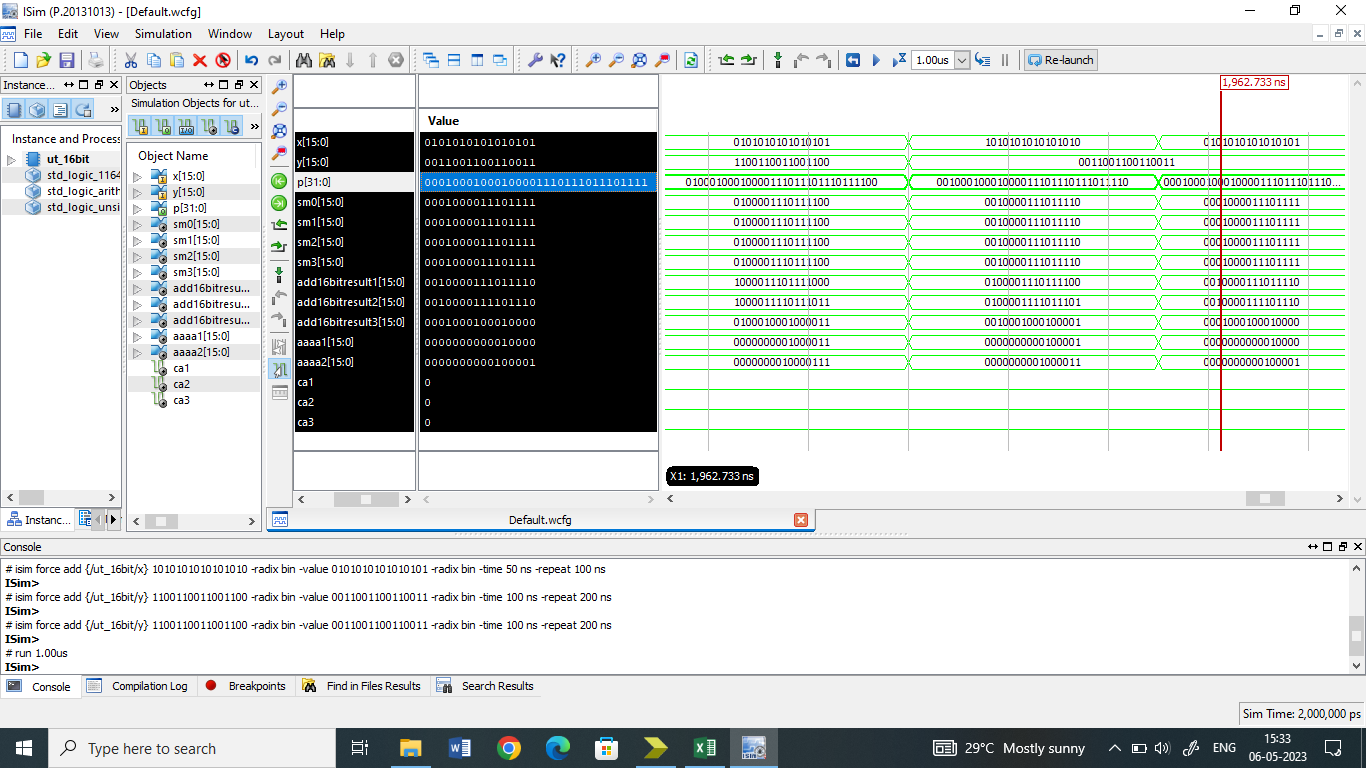


***Fig. 18:*** *Synthesis of 16×16 Bit Vedic UrdhvaTiryakbhyam Multiplier with Half and Full Adders*

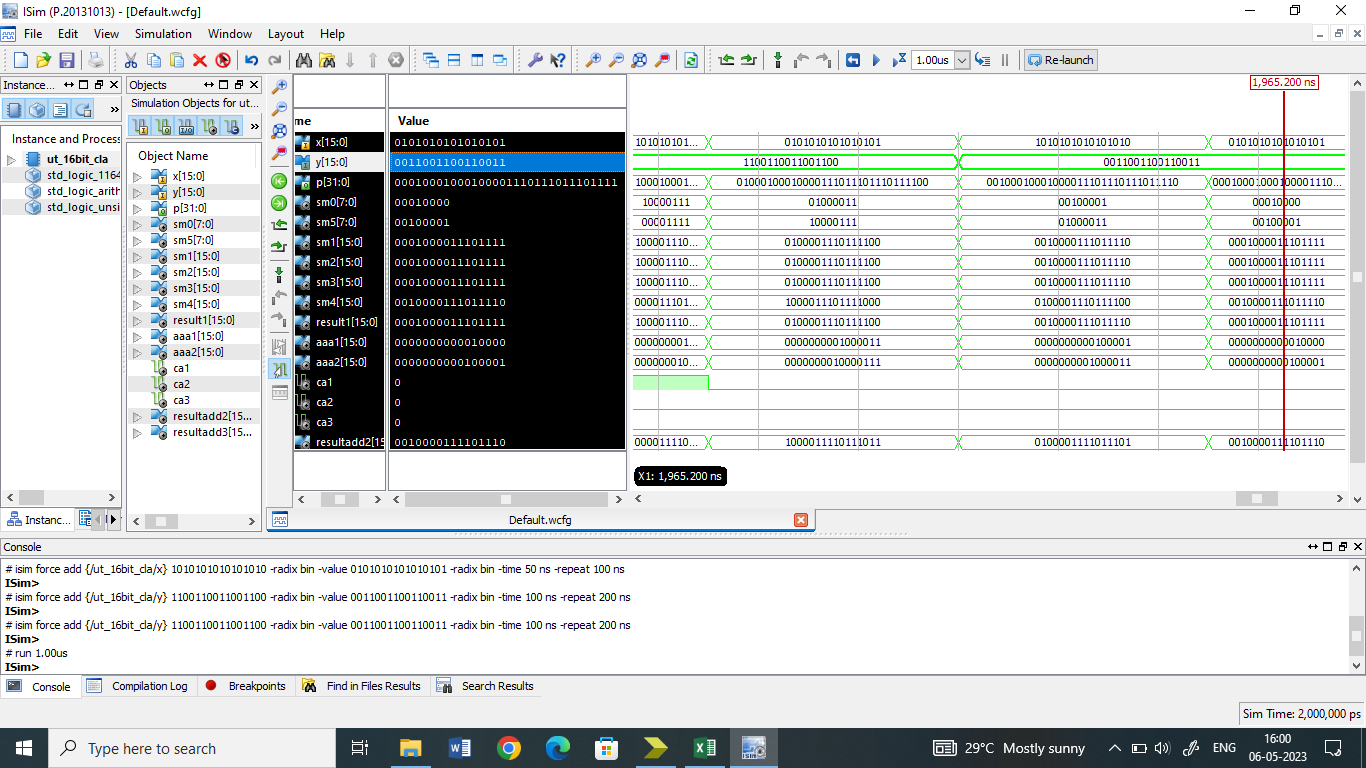
The designed VHDL code is simulated using Xilinx ISim simulator for all designs. The simulation wave form for these designs of UT Vedic multiplier with different partial product addition schemes are shown in Fig. 19 to Fig. 23.



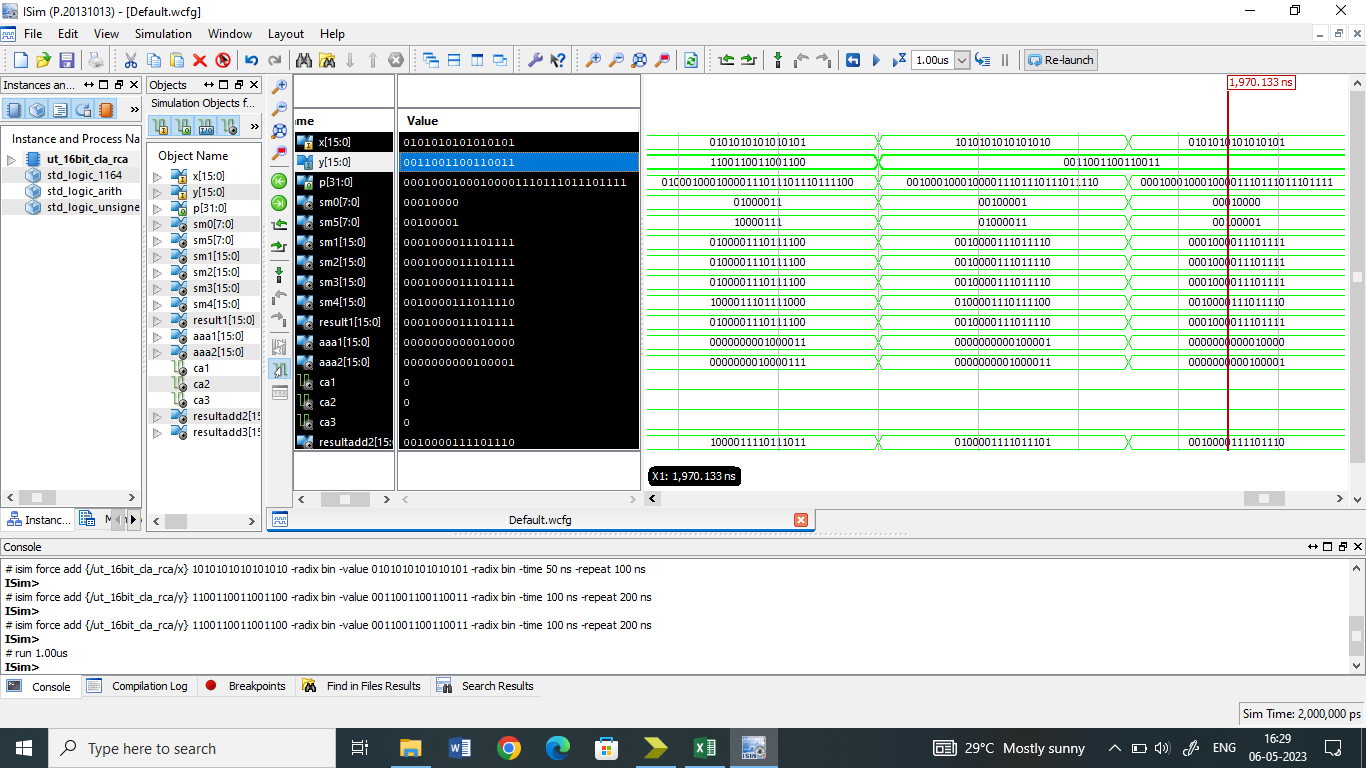
***Fig. 19:*** *Simulation of 16×16 Bit Array Multiplier*



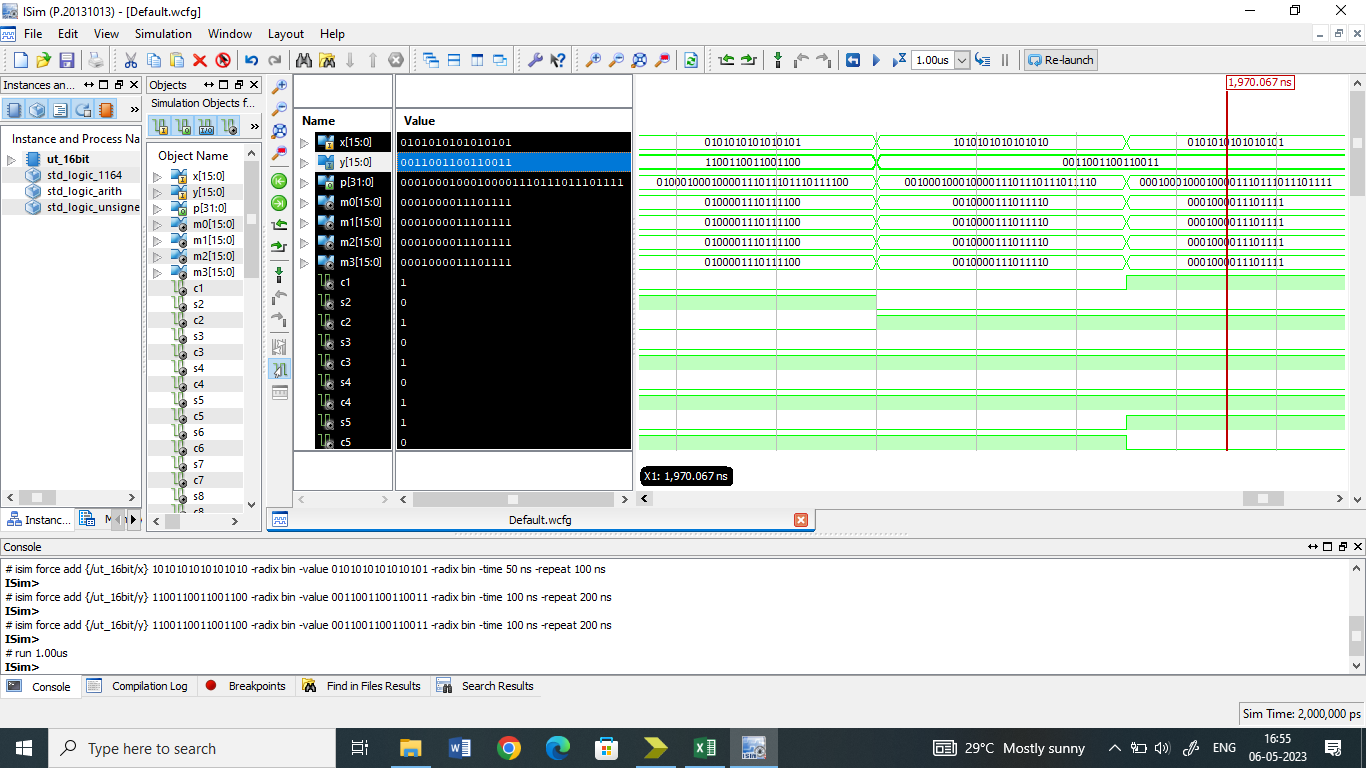
***Fig. 20:*** *Simulation of 16×16 Bit Vedic UrdhvaTiryakbhyam Multiplier with RCA*



***Fig. 21:*** *Simulation of 16×16 Bit Vedic UrdhvaTiryakbhyam Multiplier with CLA Adders*



***Fig. 22:*** *Simulation of 16×16 Bit Vedic UrdhvaTiryakbhyam Multiplier with CLARCA Adders*



***Fig. 23:*** *Simulation of 16×16 Bit Vedic UrdhvaTiryakbhyam Multiplier with Half and Full Adders*

**RESULTS :**

Synthesis of the designed multiplier was done using Xilinx ISE 14.7. and the report related to Number of Slices, Number of 4 input LUTs and delay is presented in Table 1 to Table 3. For calculation of power dissipation XPower analyzer tool is used, the switching activity data can be written at the time of simulation after place and route(PAR). This switching activity data file is used by XPower analyzer to calculate total power. The power calculations will help to optimize the power during design. In our design the simulation inputs are kept same for array and vedic multiplier so that there should be same effect of dynamic power on the circuits. The total power dissipation of each multiplier is shown in Table 1 to Table 3.

***Table 1:*** *Comparison of 4 Bit Array and UT Vedic Multiplier*

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Type of multiplier** | **Total number of Slice LUTs:** | **LUT with number of input** | | | | | **Total delay in ns** | **delay in logic** | **delay in route** | **Power (W)** |
| **2** | **3** | **4** | **5** | **6** |
| Array 4 bit | 23 | 6 | - | 4 | - | 13 | 13.263 | 5.745 | 7.518 | 0.023 |
| UrdhvaTiryakbhyam 4 bit multiplier with RCA adder | 25 | 1 | - | 12 | 6 | 6 | 12.096 | 5.491 | 6.605 | 0.021 |
| UrdhvaTiryakbhyam 4 bit multiplier with CLA adder | 24 | 3 | - | 7 | - | 14 | 13.702 | 5.764 | 7.938 | 0.023 |
| UrdhvaTiryakbhyam 4 bit multiplier with CLA RCA adder | 24 | 3 | - | 7 | - | 14 | 13.702 | 5.764 | 7.938 | 0.023 |
| UrdhvaTiryakbhyam 4 bit multiplier with Half adders and Full adders | 26 | 7 | - | 7 | - | 12 | 11.978 | 5.51 | 6.468 | 0.020 |

***Table 2:*** *Comparison of 8 Bit Array and UT Vedic Multiplier*

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Type of multiplier** | **Total number of Slice LUTs:** | **LUT with number of input** | | | | | **Total delay in ns** | **delay in logic** | **delay in route** | **Power (W)** |
| **2** | **3** | **4** | **5** | **6** |
| Array 8 bit | 93 | 12 | - | 18 | 2 | 61 | 28.043 | 8.516 | 19.527 | 0.038 |
| UrdhvaTiryakbhyam 8 bit multiplier with RCA adder | 130 | 4 | 6 | 50 | 32 | 38 | 21.052 | 7.28 | 13.772 | 0.034 |
| UrdhvaTiryakbhyam 8 bit multiplier with CLA adder | 128 | 13 | 3 | 32 | 7 | 73 | 22.236 | 7.269 | 14.967 | 0.037 |
| UrdhvaTiryakbhyam 8 bit multiplier with CLA RCA adder | 128 | 11 | 3 | 34 | 13 | 67 | 22.619 | 7.511 | 15.108 | 0.037 |
| UrdhvaTiryakbhyam 8 bit multiplier with Half adders and Full adders | 128 | 25 | 9 | 29 | 10 | 55 | 19.374 | 6.977 | 12.397 | 0.035 |

***Table 3:*** *Comparison of 16 Bit Array and UT Vedic Multiplier*

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Type of multiplier** | **Total number of Slice LUTs:** | **LUT with number of input** | | | | | **Total delay in ns** | **delay in logic** | **delay in route** | **Power (W)** |
| **2** | **3** | **4** | **5** | **6** |
| Array 16 bit | 365 | 13 |  | 92 | 8 | 252 | 55.351 | 13.539 | 41.812 | 0.066 |
| UrdhvaTiryakbhyam 16 bit multiplier with RCA adder | 578 | 17 | 28 | 204 | 155 | 174 | 38.239 | 9.543 | 23.696 | 0.062 |
| UrdhvaTiryakbhyam 16 bit multiplier with CLA adder | 632 | 56 | 23 | 139 | 56 | 358 | 35.12 | 9.763 | 25.357 | 0.067 |
| UrdhvaTiryakbhyam 16 bit multiplier with CLA RCA adder | 572 | 40 | 24 | 141 | 77 | 290 | 38.086 | 10.294 | 27.792 | 0.066 |
| UrdhvaTiryakbhyam 16 bit multiplier with Half adders and Full adders | 570 | 101 | 41 | 123 | 70 | 235 | 29.89 | 9.225 | 20.665 | 0.061 |

**CONCLUSION:**

16 bit Vedic multiplier implemented with RCA adders had a propagation delay that was 30.9% better than array multiplier but had 36.8% more slice LUTs. Carry lookahead (CLA) adders are used in place of RCA adders to further reduce delay. The propagation time was further reduced by 8.15 % as a result of this implementation with the CLA adder, but the area, or the number of slices and LUTs, increased by 8.54%. Due to the intricate circuits utilized to generate carry propagate and carry generate, the Vedic multiplier with CLA adder is faster but has incerase in slices and LUTs. For a group of four CLA addres, the RCA adder approach is utilized to simplify the circuit at the expense of compromising latency.

The outcome demonstrates that the utilization of slice LUTs is reduced in 16 bit multi with RCA CLA adder, however the technique of RCA CLA adders has little effect on delay and power. The propagation time was reduced by 45.9 % and 21.8 %, respectively, utilizing the half adder and full adder methods presented as opposed to array multiplier and vedic multiplier with RCA adders. But the propagation delay of the suggested approach is roughly equivalent to that of the vedic multiplier with CLA adders. But among all multiplier implementations, the suggested method of half adders and full addres had the lowest power dissipation. The suggested implementation requires 1.6%, 8.95%, and 7.46% less power than the vedic multiplier with RCA adders, CLA adders, and RCA CLA adders, respectively.

For the 16 × 16 bit Vedic multiplier and array multipliers, the performance parameters of the multiplier, such as delay, area, and power dissipations, were calculated. In compared to an array multiplier, it has been found that a 16-bit Vedic multiplier with half-and-full adders and carry lookahead adders performs roughly 45.9 % and 36.5% faster, respectively. The suggested method of half adders and full adders is a preferable option for addition of partial products if a slight increase in propagation delay is allowed at the expense of reduced area, i.e. slices and LUTs. Additionally, the proposed technique uses less power than all other implementations. Vedic multiplier is used for fast multiplication at the same time if there is need of small area and less power the proposed method is a better alternative for addition of partial products.

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